Structural investigation of SiGe/Ge superlattices for thermoelectric applications


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Thermoelectric phenomena involve the conversion between thermal and electrical energy and provide a method for heating and cooling materials. Thermoelectricity is expected to play an increasingly important role in meeting the energy challenge of the future, especially by exploiting waste heat from other processes. Thus quite a substantial effort is devoted worldwide on the development of advanced thermoelectric materials for many different applications.

The effectiveness of a thermoelectric material can be linked to the dimensionless thermoelectric figure of merit \( ZT \), where \( S \), \( \sigma \), \( T \), and \( \kappa \) are, respectively, the Seebeck coefficient, electrical conductivity, temperature, and thermal conductivity [1]. Thus high performance thermoelectric materials require high Seebeck coefficient, high electrical and low thermal conductivity. In the last years, the focus of research has been both on advanced bulk thermoelectric materials, and on low dimensional systems in which the carrier transport is confined to less than three dimensions, i.e., nanostructures like multiquantum well structures, quantum wires and quantum dots. In this second class of materials the confinement is used to enhance the power factor \( S^2\sigma \) whereas the large number of interfaces in these nanostructures has to be designed to reduce the thermal conductivity \( \kappa \) and at the same time to keep the electrical conductivity \( \sigma \) as high as possible. This can be achieved by tailoring the corresponding scattering lengths [2, 3].

One promising suggestions for thermoelectric applications, in particular for integrated on-chip energy harvesting, consists in the use of Si/SiGe nanostructures because of their compatibility with mature Si technology. For improving the figure of merit \( Z \) one has to design the electronic band structure e.g. of a multiquantumwell structure or a superlattice properly, but at the same time introduce barriers for phonon transport, i.e., to ensure that scattering by the interfaces reduces the thermal transport more effectively than the electrical one. Another possibility offered by multiquantum wells and superlattices is the appearance of phonon band gaps affecting the thermal transport as well. One such proposed device design made from a superlattice structure with vertical transport direction is visualized in Fig. 1.

In such superlattices, the interface roughness and its vertical and lateral correlations are crucial both for determining the electrical as well as the thermal conductivity. Due to the 4.2% lattice mismatch between Si and Ge one has to ensure strain symmetrization within the superlattice stack. Due to the material properties of Ge, high Ge contents is advantageous for a high thermoelectric figure of merit, typically average Ge contents of about 80% are used. To avoid further misfit dislocations within the superlattice stack, it has to be deposited on a relaxed SiGe buffer layer with proper composition. At the interface between the buffer layer and the Si, misfit dislocations ensure that the buffer is relaxed, while threading dislocation segments are present in the whole SL stack. Simulations of their influence on the electrical

Figure 1: Designed thermoelectric on-chip generator with SiGe/Ge superlattice in vertical transport direction.
transport demonstrate that up to densities of about $10^7 \text{ cm}^{-2}$ their impact is negligible, which holds for the phonon transport as well.

We investigated structural properties of SiGe/Ge superlattices, especially the influence of growth conditions on interface roughness and roughness correlation. While dislocations were characterized by X-ray diffraction (XRD) and transmission electron microscopy (TEM), for the interface roughness and correlations X-ray reflectivity (XRR) and grazing incidence X-ray scattering (GISAXS) were the methods of choice.

We performed XRD and XRR measurements at beamline P08 and GISAXS experiments at beamline BW4 in order to characterize the layers together with the interface roughness and also the roughness correlation. The measured reciprocal space maps are compared with calculated and optimized ones as visualized in Fig. 2. By this method the thickness and composition of the layer together with the integral r.m.s. roughness, the Hurst parameter and the lateral and vertical correlation lengths of the interfaces are determined [4].

In order to reproduce the measured intensity fluctuations in the layer thicknesses and also variations in the thickness duty cycle of the SiGe/Ge bilayer had to be introduced. We found duty cycle changes up to 11 % of the mean period while the period itself stayed very very constant with a variation of less then 1 %.

![XRD radial scan around the (004) Si Bragg peak (red line) together with the simulated curve (blue line) of a 10 period SiGe/Ge superlattice test sample.](image)

![XRR map around the origin of reciprocal space (coloured data) overlayed with simulated data (black lines) of a 50 period SiGe/Ge superlattice.](image)

Figure 2: XRD and XRR measurements together with simulations.

These findings are corroborated by TEM studies and electrical and thermal transport measurements will follow. So far the homogeneity of the samples is not sufficient in order to form the mentioned minibands. The found results are therefore used to optimize growth and design towards the proposed nanostructures tailored for on-chip thermoelectric energy generators.

References