Reflectometric and Topographic Studies of the Influence of Surface Preparation on SiC Epitaxial Layers Growth


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The technology of modern high temperature electronic materials often includes the deposition of homoepitaxial silicon carbide layers. Deposition of perfect epitaxial layers is even more dependent on the appropriate finishing of the surface, than on the concentration of the defects in the substrate crystals. X-ray reflectometric and diffraction topographic methods were applied for examination of 4H and 6H silicon carbide substrates finished with various regimes as well as silicon carbide epitaxial layers.

The X-ray reflectometric investigation were performed for a number of samples both of 4H and 6H SiC polytypes prepared using finishing regimes developed at the Institute of Electronic Materials Technology (IEMT). The structural perfection of the epitaxial layers and the substrate wafers was also controlled by synchrotron X-ray diffraction topography realized both in white and monochromatic beam.

The values of the surface roughness were evaluated by fitting of the theoretical reflectivity curves to the experimental ones, by means of REFSIM program. The obtained X-ray reflectivity curves for 8° and 0° off-cut 4H SiC substrates are presented in Fig. 1. The values of surface roughness σ evaluated from the best fit theoretical curves are slightly higher than 2nm, namely σ = 2.09±0.05nm for 4H SiC wafer with 0° off-cut and σ = 2.16±0.05nm for 6H SiC with 8° off-cut respectively.

![Figure 1: The measured and simulated X-ray ref. curves for substrate wafers manufactured by SiCrystal with 8° off-cut and the evaluated roughness σ = 2.16±0.05 nm and with 0° off-cut (on axis) and the evaluated roughness σ = 2.06±0.05nm, respectively.](image-url)
In order to receive perfect epitaxial layer the improved finishing process of the substrate surface (i) and the new pre-etching process before the epitaxial process (ii) were established at IEMT. Applying of more fine surface lapping decreased the surface roughness up to 0.85 nm for 6H SiC with 4° off-cut. This value was close to the surface roughness of the 6H SiC on axis substrates manufactured by Cree Inc. Additional finishing with electrochemical treatment (ECMP) used to the 4H SiC sample from the Institute of Electronic Materials Technology with 8° off-cut resulted in surface roughness $\sigma = 0.55$nm.

On the 4HSiC substrate wafer with 8° off-cut manufactured at IEMT the 20 µm-thick epitaxial layer was deposited after pre-etching process. The evaluated value of the surface roughness was $\sigma = 1.14 \pm 0.05$ nm.

The synchrotron white beam projection (a) and section (b) topographs of the sample are shown in Fig. 2 indicating a relatively good perfection of the layer, shown by of individual dislocations and some pipe-formed cavities. It should be, however, noted that the PVD generator used at the Institute of Electronic Materials Technology provide crystals containing higher concentration of defects than in the case of crystals grown by SiCrystal and Cree Inc.

Figure 2: Synchrotron white beam projection – a. and section – b topographs of the sample 4H SiC with 8° off-cut finished by means of electrochemical treatment (ECMP) with 20µm-thick SiC epitaxial layer manufactured at the Institute of Electronic Materials Technology.